AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) ~~The data transmitting/receiving device of claim 1,~~ A data transmitting/receiving device, comprising:

a serial-parallel conversion circuit for converting received first serial data to first parallel data;

a data selection circuit for selecting any one of the first parallel data and externally-supplied second parallel data and outputting the selected data; and

a parallel-serial conversion circuit for converting the first or second parallel data output from the data selection circuit to second serial data which is to be transmitted,

wherein the parallel-serial conversion circuit receives a common clock signal with the serial-parallel conversion circuit and operates in synchronization with ~~the serial-parallel circuit~~ the common clock signal when the data selection circuit selects the first parallel data.

3. (Currently Amended) The data transmitting/receiving device of claim [[1]] 2, further comprising a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data,

wherein the serial-parallel conversion circuit operates in synchronization with the second clock signal.

4. (Original) The data transmitting/receiving device of claim 2, further comprising a clock selection circuit for selecting any one of the first clock signal and the second clock signal and inputting the selected clock signal to the parallel-serial conversion circuit, wherein:

when the data selection circuit selects the first parallel data, the clock selection circuit

selects the second clock signal; and

when the data selection circuit selects the second parallel data, the clock selection circuit selects the first clock signal.

5. (Cancelled)

6. (Currently Amended) ~~The data transmitting/receiving device of claim 5,~~ A data transmitting/receiving device, comprising:

a serial-parallel conversion circuit for converting received first serial data to first parallel data;

a data processing circuit for outputting second parallel data;

a control circuit for stopping the operation of the data processing circuit;

a data selection circuit for selecting any one of the first parallel data and the second parallel data and outputting the selected data; and

a parallel-serial conversion circuit for converting the first or second parallel data output from the data selection circuit to serial data which is to be transmitted,

wherein the parallel-serial conversion circuit receives a common clock signal with the serial-parallel circuit and operates in synchronization with ~~the serial-parallel circuit~~ the common clock signal when the data selection circuit selects the first parallel data.

7. (Original) The data transmitting/receiving device of claim 6, further comprising a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data,

wherein the serial-parallel conversion circuit operates in synchronization with the second

clock signal.

8. (Original) The data transmitting/receiving device of claim 7, further comprising a clock selection circuit for selecting any one of the first clock signal and the second clock signal and inputting the selected clock signal to the parallel-serial conversion circuit, wherein:

when the data selection circuit selects the first parallel data, the clock selection circuit selects the second clock signal; and

when the data selection circuit selects the second parallel data, the clock selection circuit selects the first clock signal.

9. (Original) The data transmitting/receiving device of claim 7, wherein:

the data processing circuit is divided into a plurality of units, the distances of the plurality of units from the clock adjustment circuit being different from each other; and

the control circuit stops the operation of the data processing circuit independently for each of the units.

10. (Original) The data transmitting/receiving device of claim 8, wherein:

the data processing circuit is divided into a plurality of units, the distances of the plurality of units from the clock adjustment circuit being different from each other; and

the control circuit stops the operation of the data processing circuit independently for each of the units.

11. (Cancelled)

12. (Currently Amended) ~~The data transmitting/receiving device of claim 11, further comprising~~ A data transmitting/receiving device, comprising:

a latch circuit for storing received first serial data;

a serial-parallel conversion circuit for converting the first serial data to first parallel data;

a parallel-serial conversion circuit for converting externally-supplied second parallel data to second serial data;

a data selection circuit for selecting any one of the first serial data and the second serial data and outputting the selected data as transmission data; and

a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data,

wherein the latch circuit and the serial-parallel conversion circuit operate in synchronization with the second clock signal.

13. (Cancelled)

14. (Currently Amended) ~~The data transmitting/receiving device of claim 13, further comprising~~ A data transmitting/receiving device, comprising:

a latch circuit for storing received first serial data;

a serial-parallel conversion circuit for converting the first serial data to first parallel data;

a data processing circuit for outputting second parallel data;

a control circuit for stopping the operation of the data processing circuit;

a parallel-serial conversion circuit for converting the second parallel data to second serial data;

a data selection circuit for selecting any one of the first serial data and the second serial

data and outputting the selected data as transmission data; and

a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data,

wherein the latch circuit and the serial-parallel conversion circuit operate in synchronization with the second clock signal.

15. (Currently Amended) The data transmitting/receiving device of claim [[13]] 14, wherein when the control circuit stops the data processing circuit, the parallel-serial conversion circuit and the serial-parallel conversion circuit stop their operation.

16. (Original) The data transmitting/receiving device of claim 14, wherein when the control circuit stops the data processing circuit, the parallel-serial conversion circuit and the serial-parallel conversion circuit stop their operation.

17. (Original) The data transmitting/receiving device of claim 14, wherein:

the data processing circuit is divided into a plurality of units, the distances of the plurality of units from the clock adjustment circuit being different from each other; and

the control circuit stops the operation of the data processing circuit independently for each of the units.

18. (Original) The data transmitting/receiving device of claim 17, wherein when the control circuit stops at least one of the plurality of units, the parallel-serial conversion circuit and the serial-parallel conversion circuit stop their operation.